**In the Claims:**

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) A testing ~~architecture~~ system for a semiconductor memory device, used for testing the semiconductor memory device, the testing architecture comprising:

a microprocessor, wherein when a start signal is received by the microprocessor, a clock signal is output from the microprocessor and transmitted to the semiconductor memory device so that a data storing signal is output from the semiconductor memory device to the microprocessor, wherein when the data storing signal is received ~~by the microprocessor~~, the data storing signal is tested, and compared by the microprocessor, and a testing result signal is output; and

a result sorting and display device, used to output the start signal to the microprocessor, receive the result signal, and sort the result signal so as to display whether data stored by the semiconductor memory device is correct,

wherein, the data storing signal is tested and compared by the microprocessor simultaneously in a time interval allocated for the clock signal being transmitted from the microprocessor to the semiconductor memory device.

2. (currently amended) The testing system ~~architecture of the semiconductor memory device~~ according to claim 1, wherein the microprocessor has a function of receiving serial data, and testing and comparing the data.

**Claim 3. (cancelled).**

4. (currently amended) A testing ~~architecture~~ system for a semiconductor memory device, used for testing the semiconductor memory device, the testing architecture comprising:

a microprocessor, wherein when a start signal is received by the microprocessor, a clock signal is output from the microprocessor and transmitted to the semiconductor memory device so as to output a data storing signal in series from the semiconductor memory device to the microprocessor, wherein when the data storing signal is received in series by the microprocessor, the data storing signal is tested, compared, and a testing result is output through a result signal; and

a result sorting and display device, used to output the start signal to the microprocessor, receive the result signal, and sort the result signal so as to display if data stored by the semiconductor memory device is correct~~,~~.

wherein, the data storing signal is tested and compared by the microprocessor simultaneously in a time interval allocated for the clock signal being transmitted from the microprocessor to the semiconductor memory device.

**Claim 5. (cancelled).**